

FIG. 1

2/44

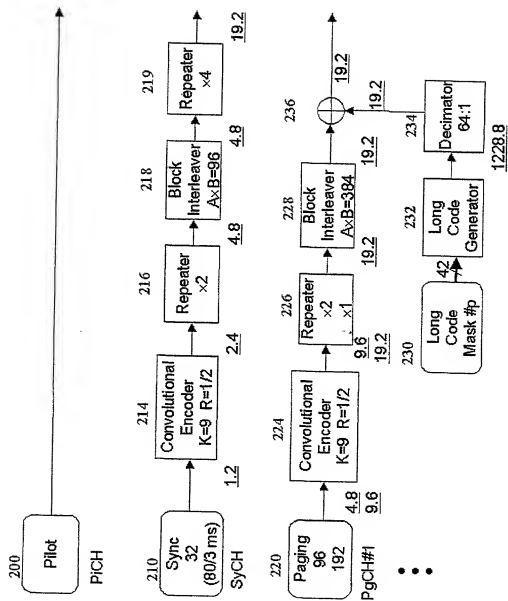


FIG. 2a

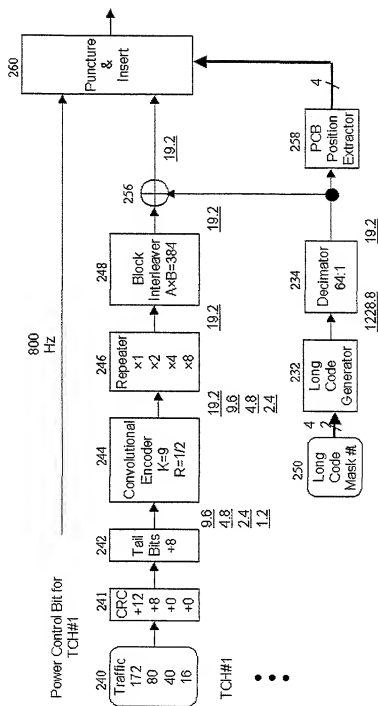


FIG. 2b

4/44

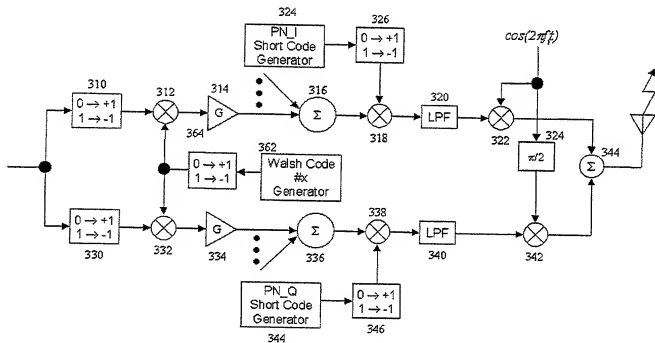


FIG. 3a

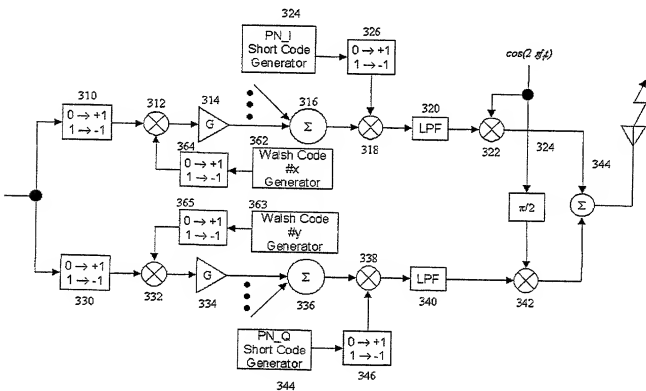


FIG. 3b

5/44

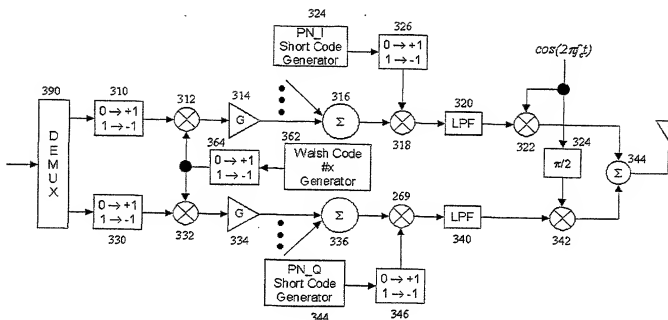


FIG. 3c

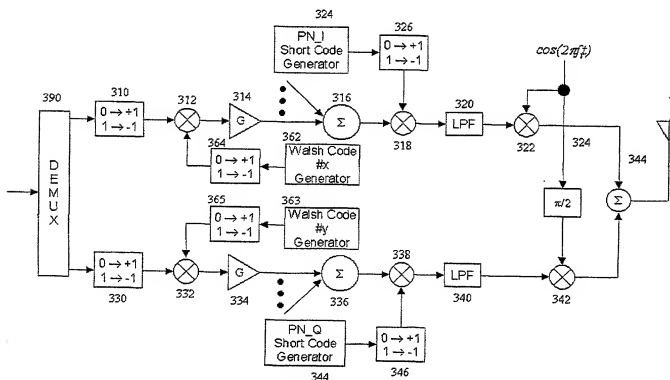


FIG. 3d

6/44

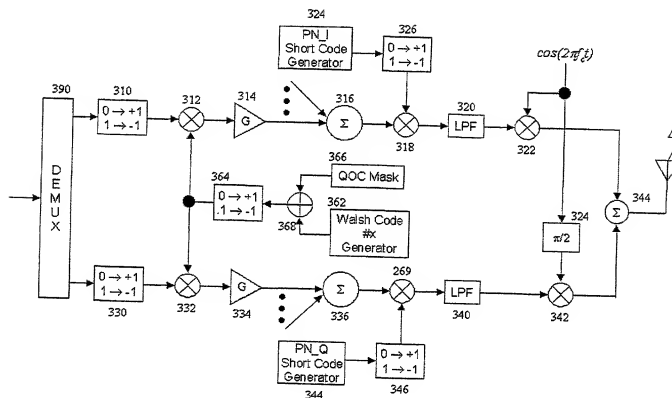


FIG. 3e

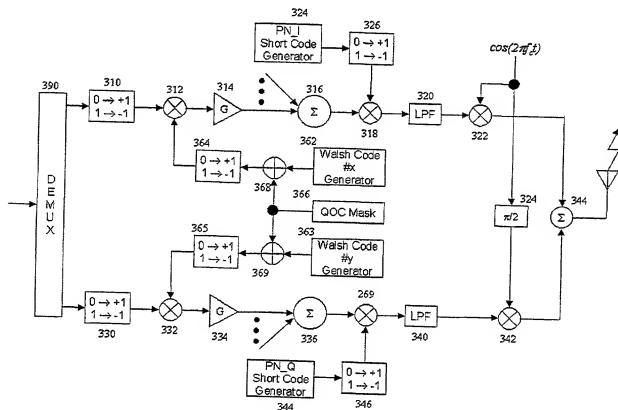


FIG. 3f

7/44

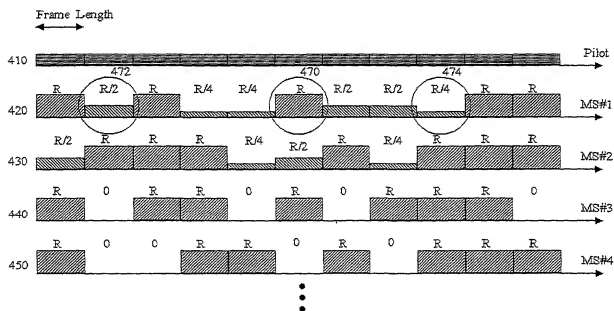


FIG 4a

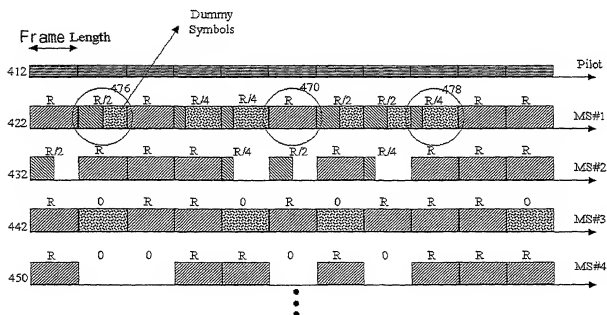


FIG. 4b

8/44

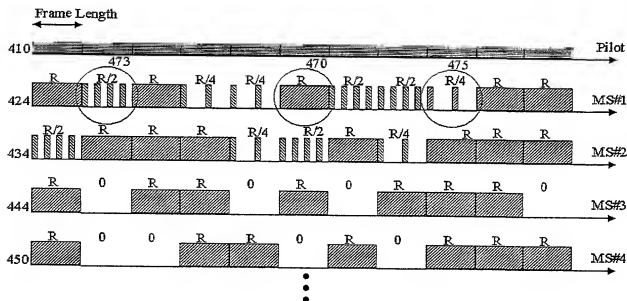


FIG. 4c

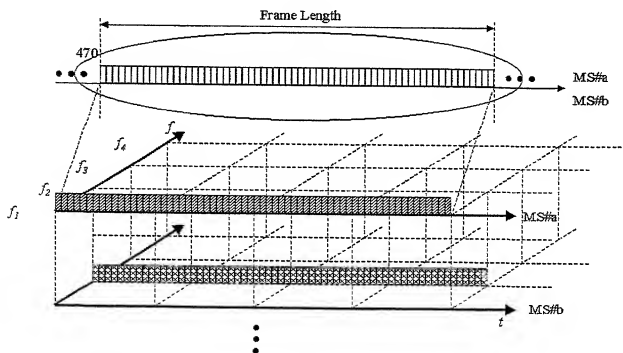


FIG. 4d



9/44

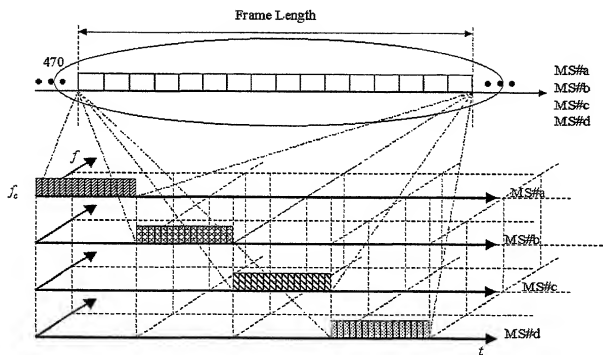


FIG. 4e

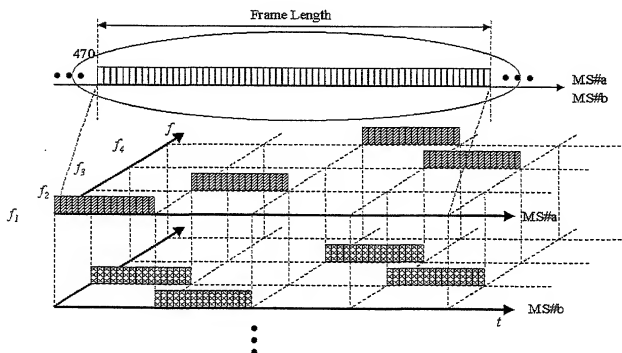


FIG. 4f

10/44

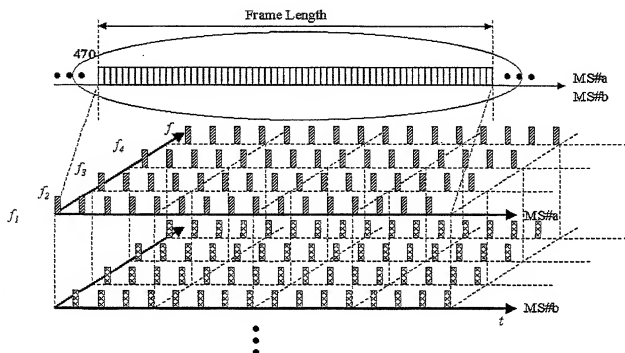


FIG. 4g

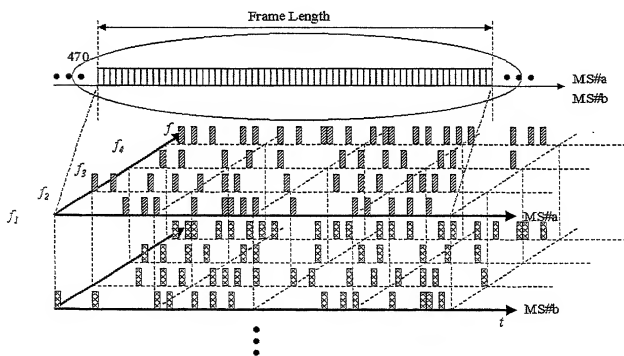


FIG. 4h

11/44

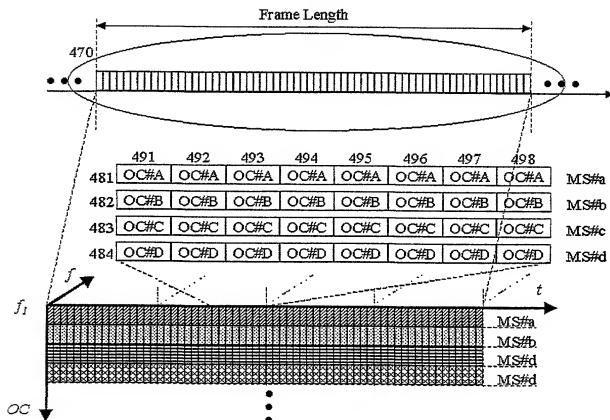


FIG. 4i

The diagram illustrates the receiver architecture for the proposed LDPC code. The process begins with an input signal (610) entering a MUX (614). The MUX also receives a feedback signal from the multiplier (618). The output of the MUX (614) is a signal (616) that passes through a Soft decision block. The Soft decision block outputs a signal (19.2) to a multiplier (618). The multiplier (618) also receives a signal (624) from a Decimator (64:1). The Decimator (64:1) receives a signal (622) from a Long Code Generator. The Long Code Generator receives a signal (620) from a Long Code Mask #p. The output of the multiplier (618) is fed back to the input of the MUX (610).

FIG. 6

13/44

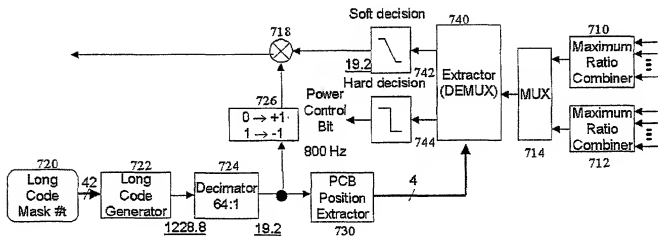


FIG. 7

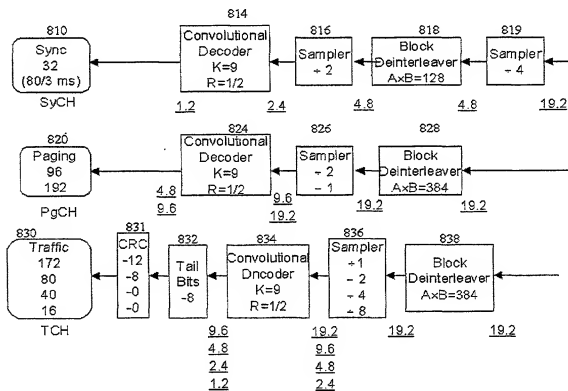


FIG. 8

14/44

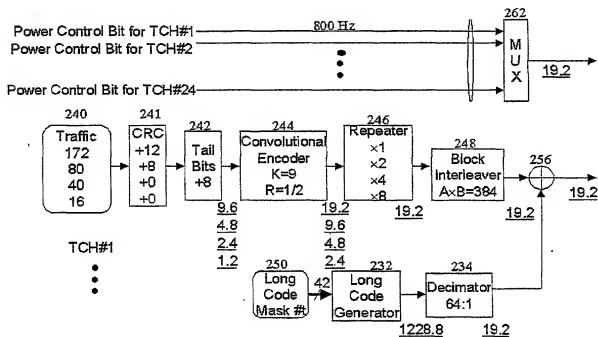


FIG. 9a

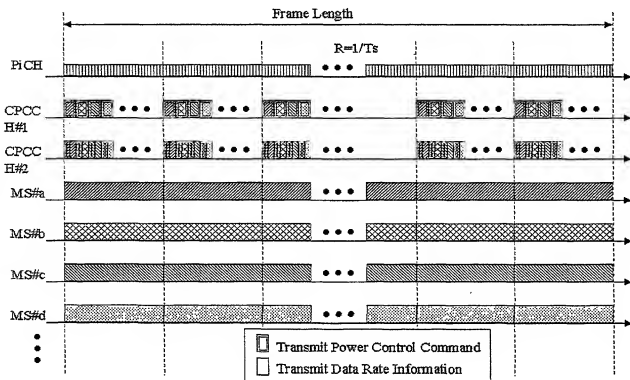


FIG. 9b

15/44

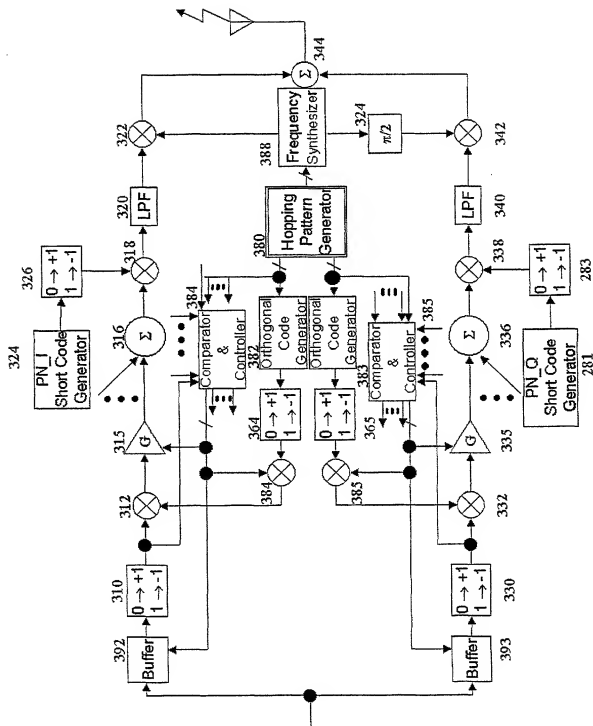


FIG. 10a

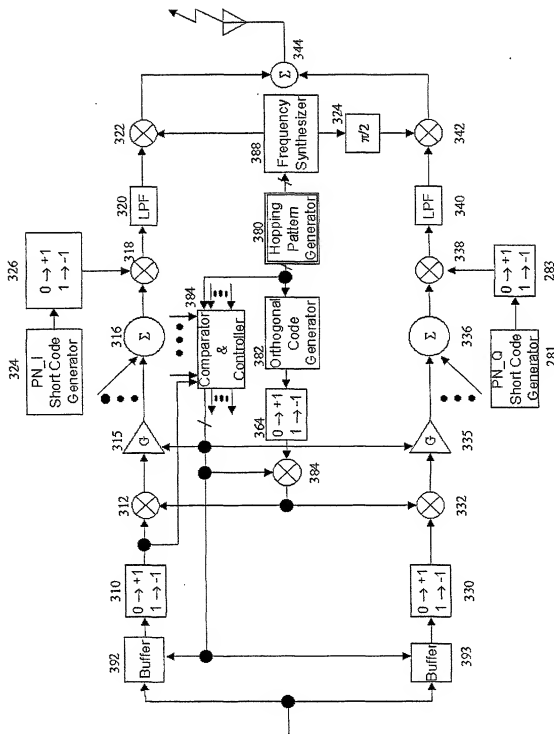


FIG. 10b



17/44

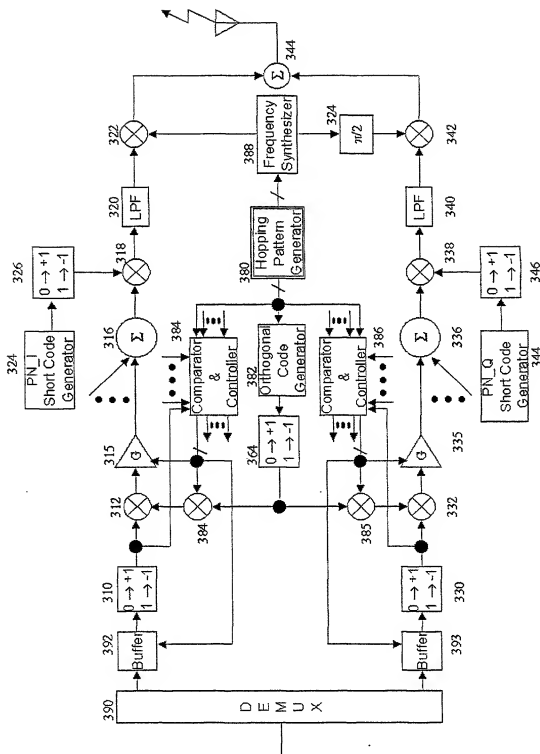


FIG. 10c

18/44

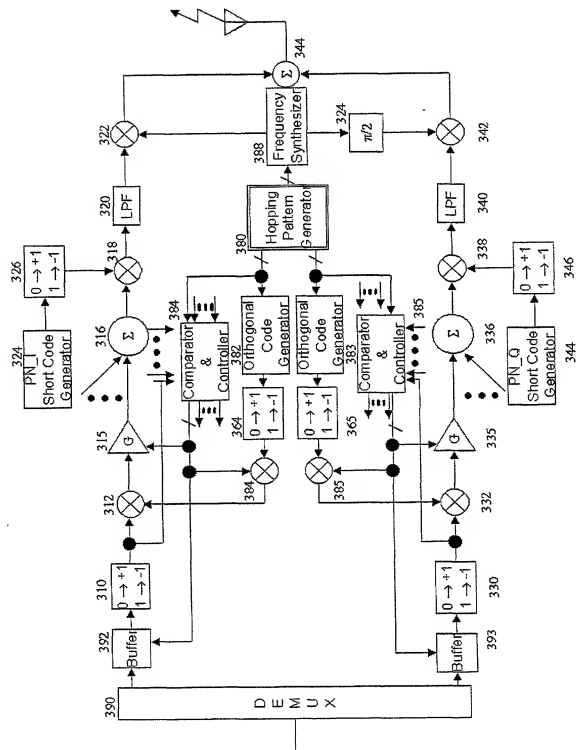


FIG. 10d

19/44

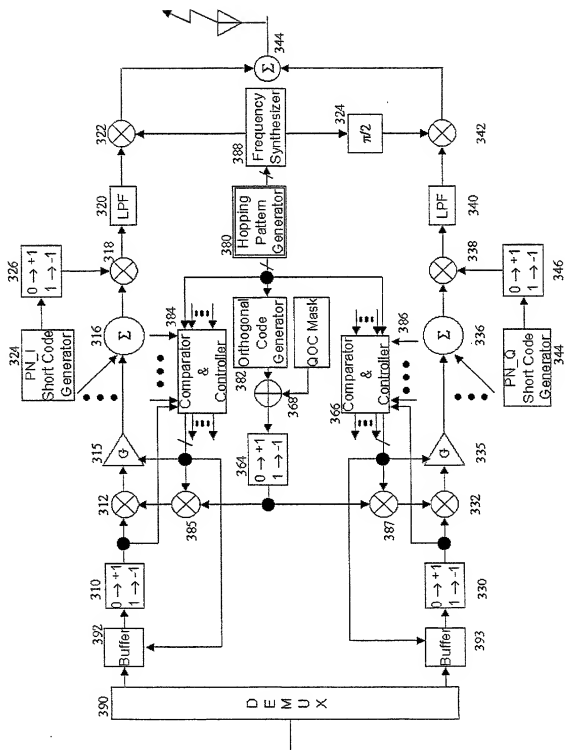


FIG. 10e

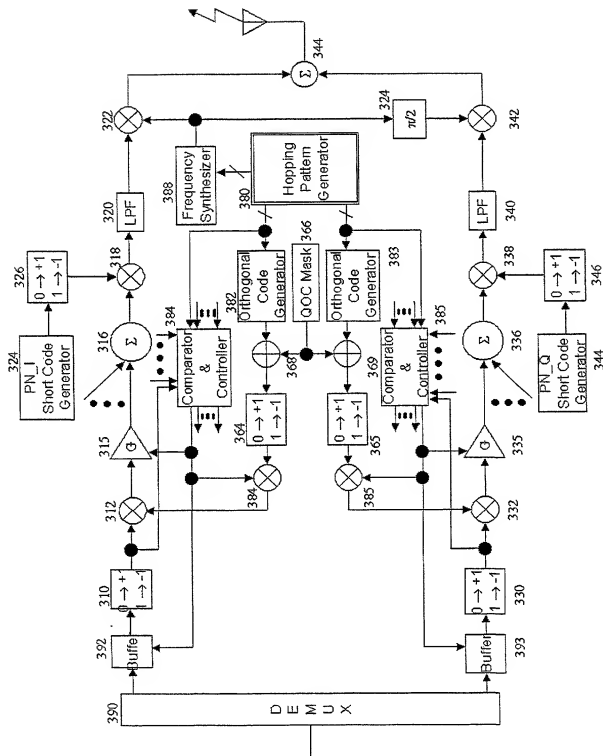


FIG. 10f

21/44

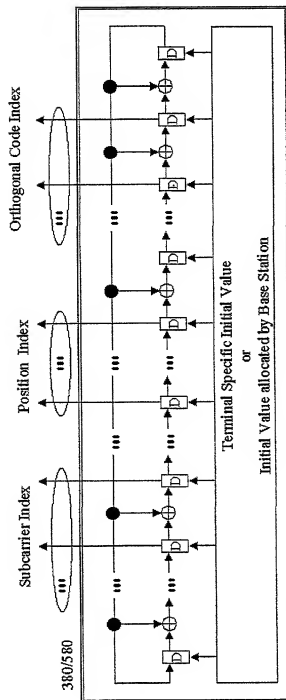


FIG. 11

22/44

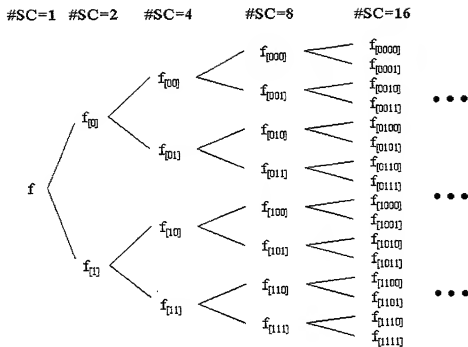


FIG. 12a

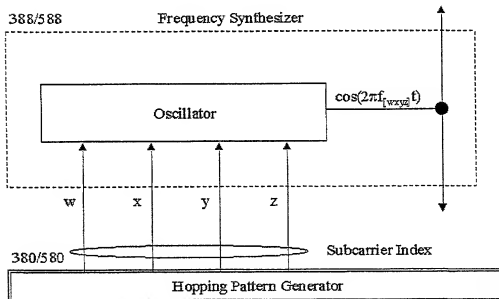


FIG. 12b

23/44

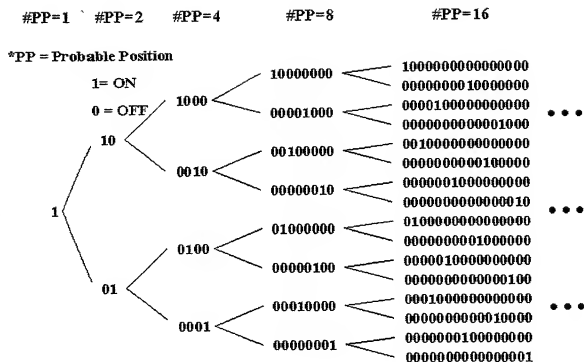


FIG. 12c

24/44

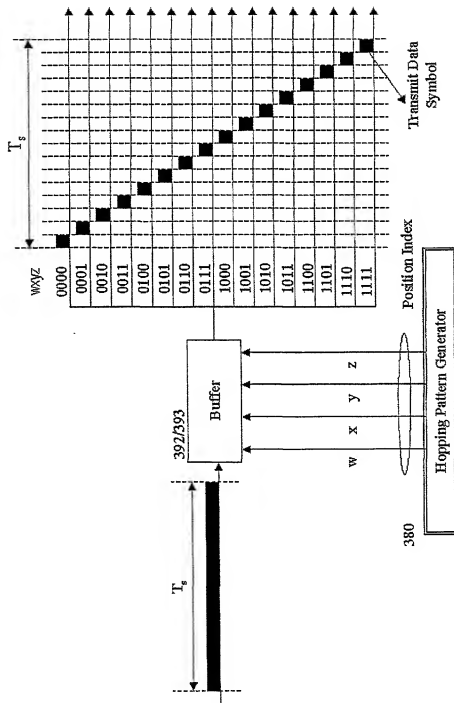


FIG. 12d



25/44

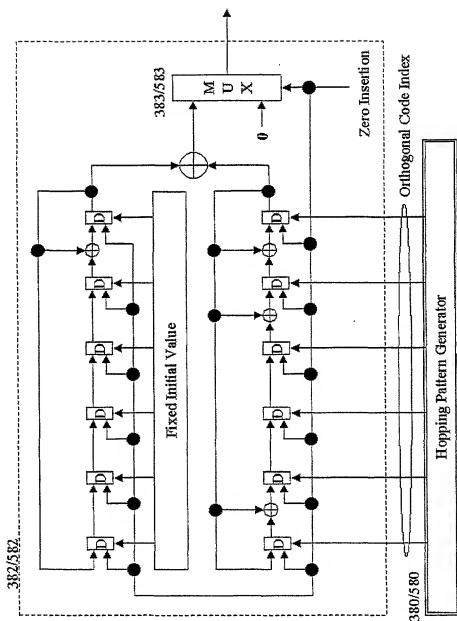


FIG. 12e

26/44

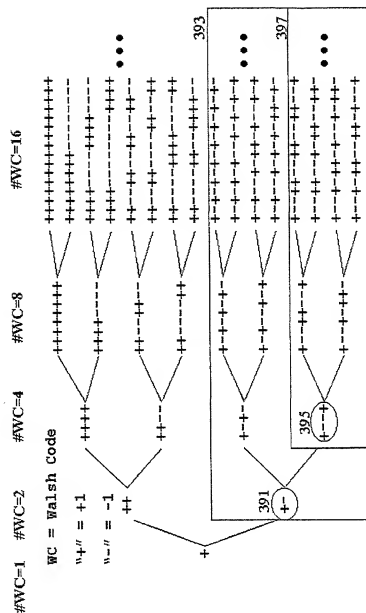


FIG. 12f

27/44

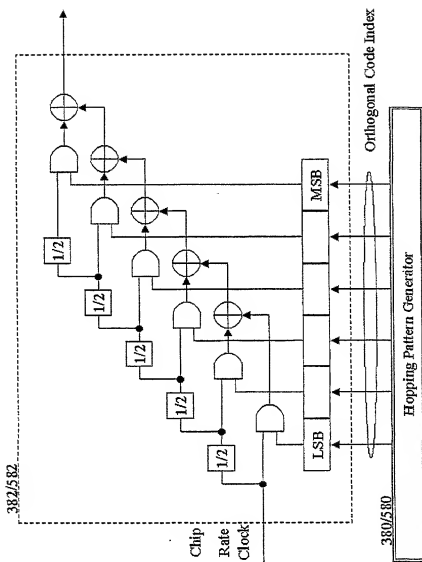


FIG. 12g

28/44

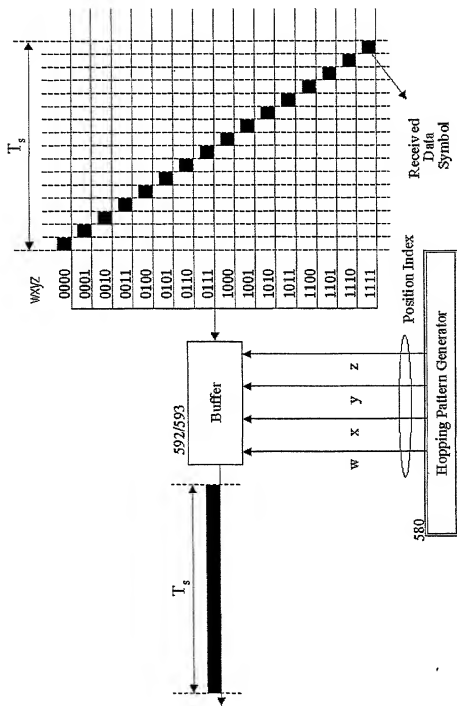


FIG. 12h

29/44

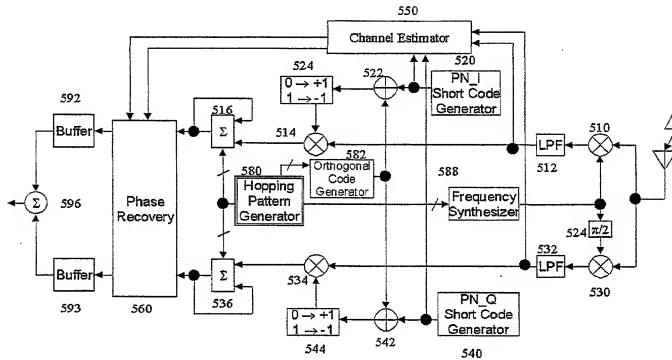


FIG. 13a

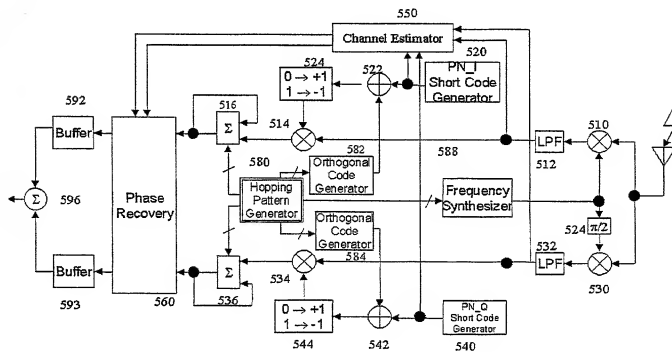
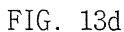
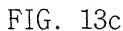


FIG. 13b



31/44

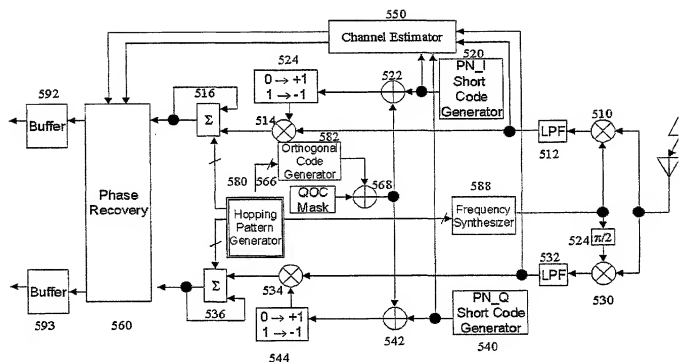


FIG. 13e

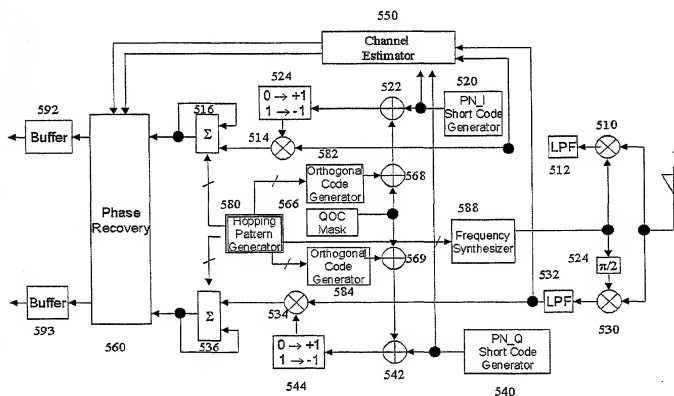


FIG. 13f

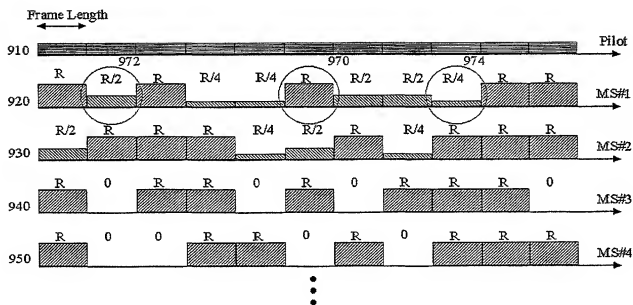


FIG. 14a

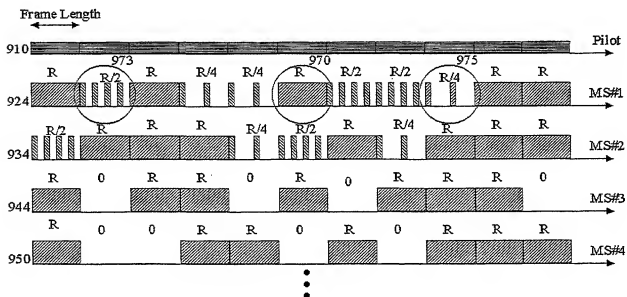


FIG. 14b



33/44

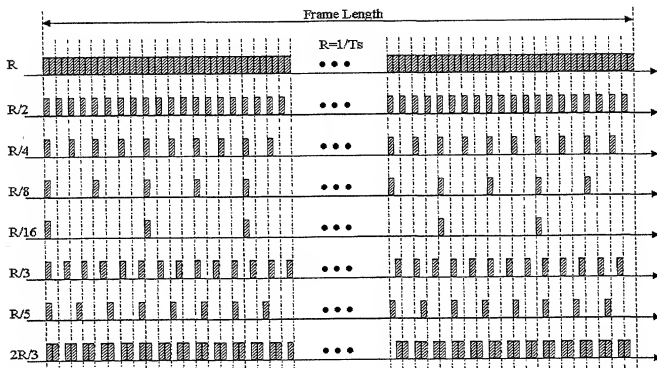


FIG. 14C

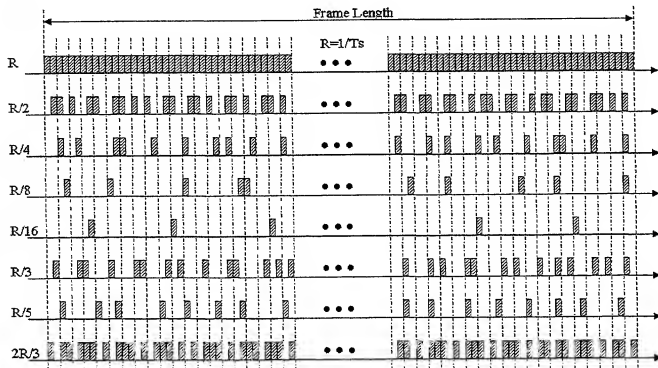


FIG. 14d

34/44

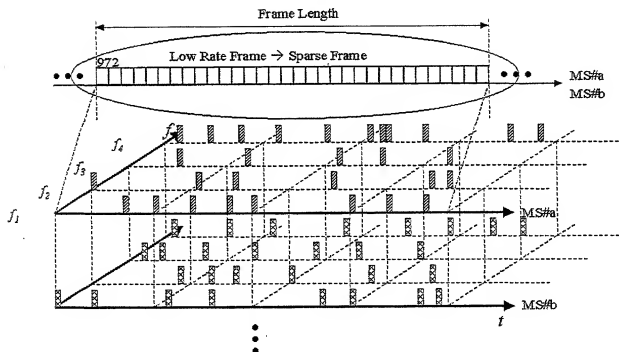


FIG. 14e

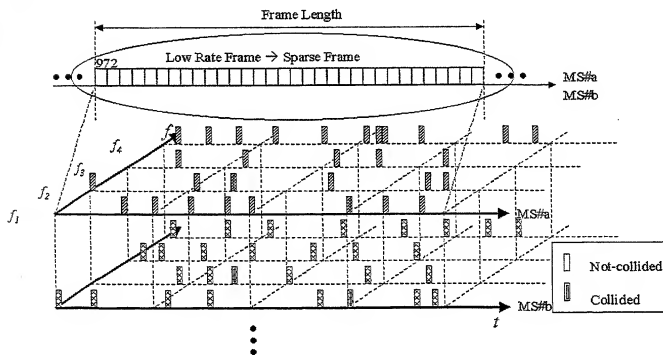


FIG. 14f

35/44

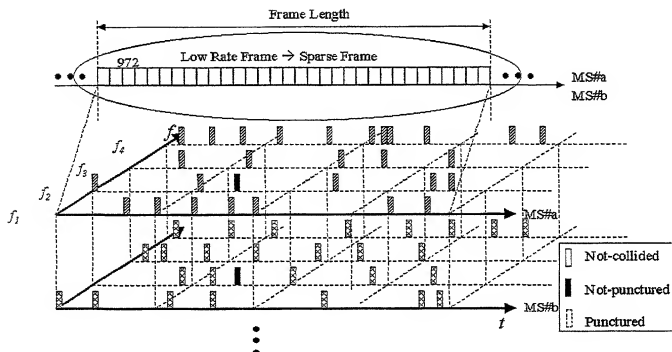


FIG. 14g

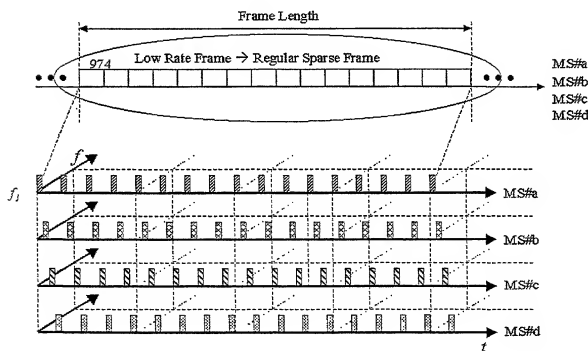


FIG. 14h

36/44

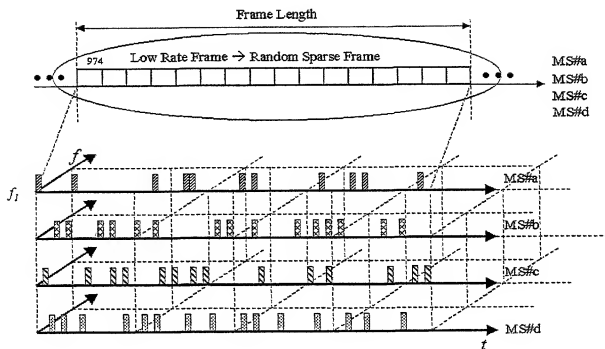


FIG. 14i

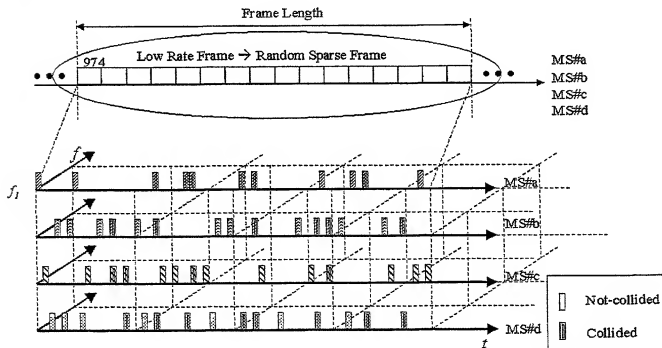


FIG. 14j

37/44

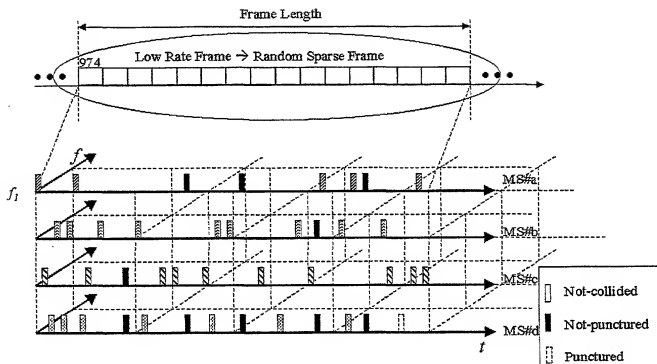


FIG. 14k

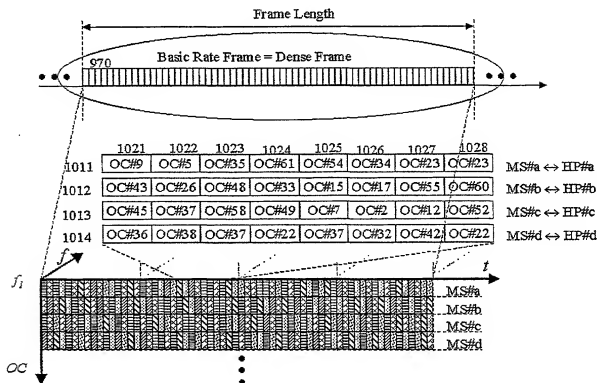


FIG. 14l

38/44

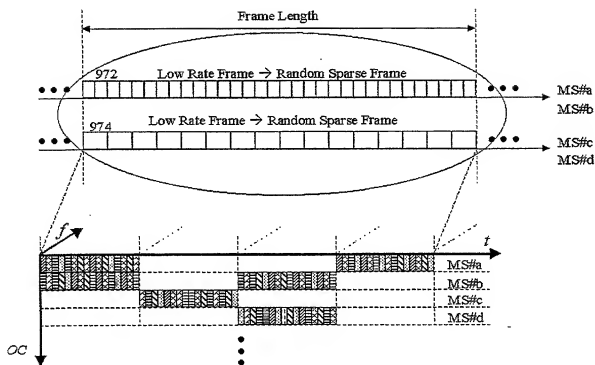


FIG. 14m

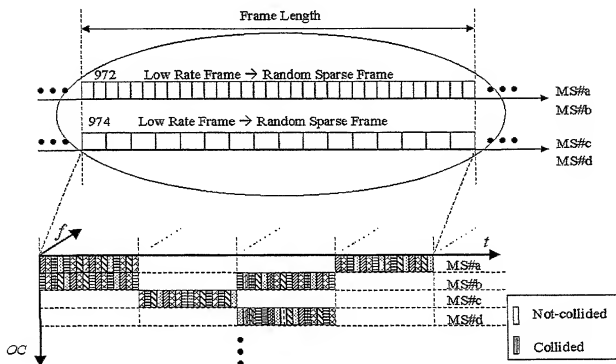


FIG. 14n

39/44

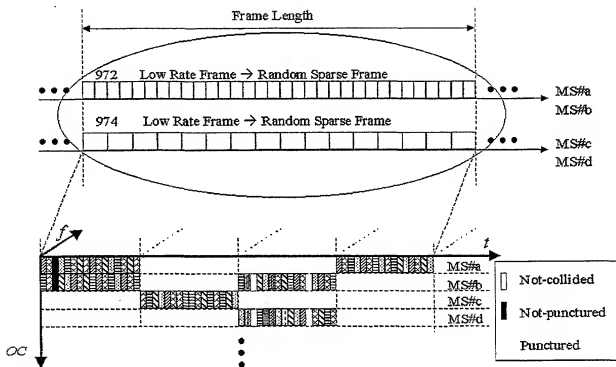


FIG. 14o

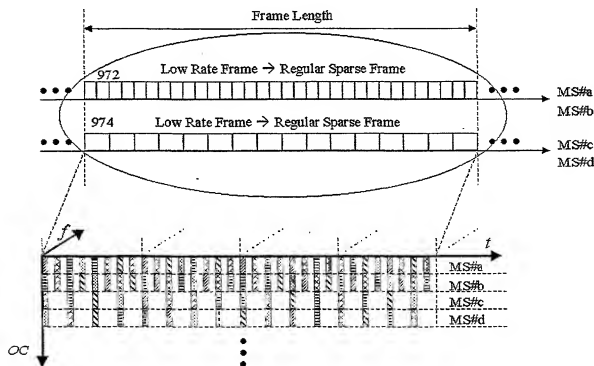


FIG. 14n

40/44

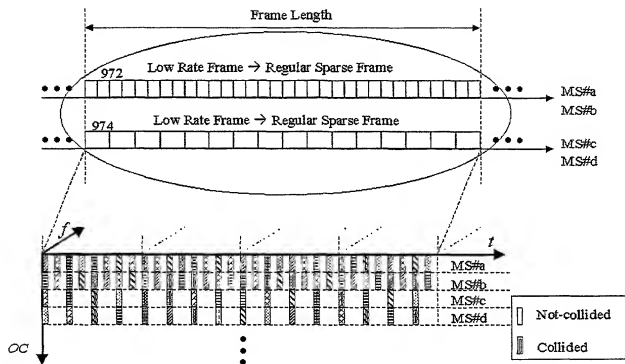


FIG. 14q

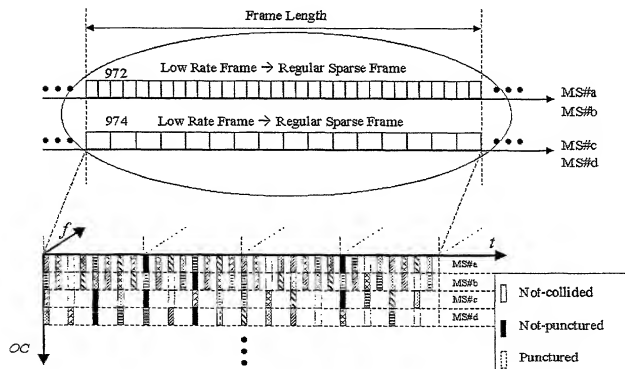


FIG. 14r



41/44

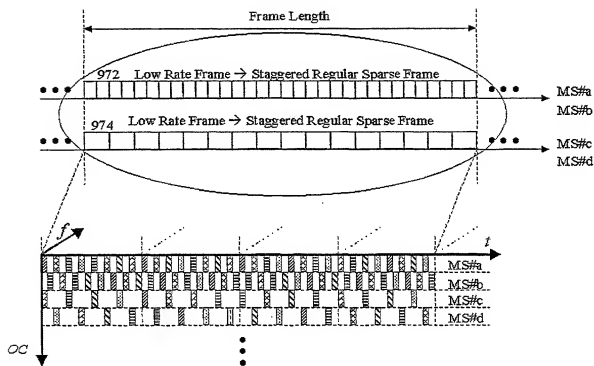


FIG. 14s

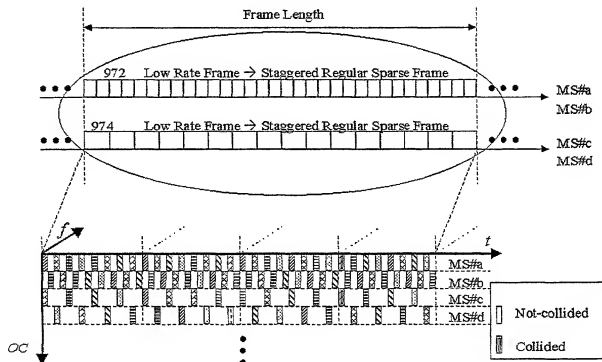


FIG. 14t

42/44

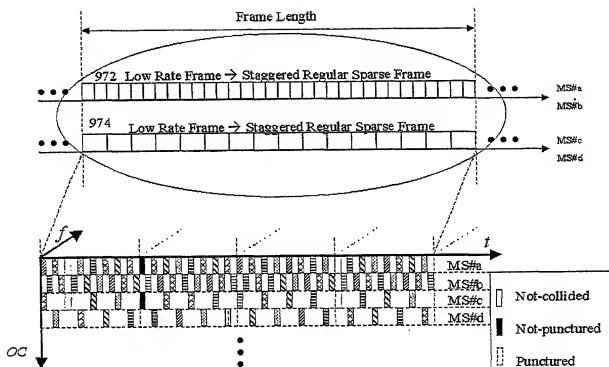


FIG. 14u

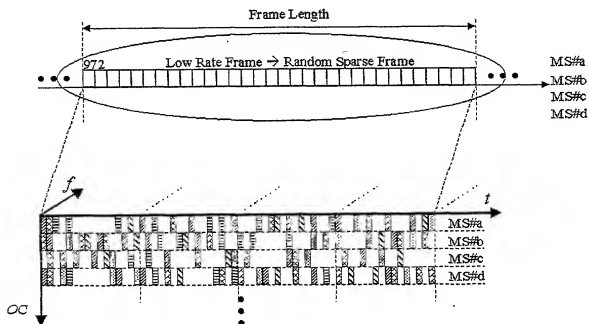


FIG. 14v

43/44

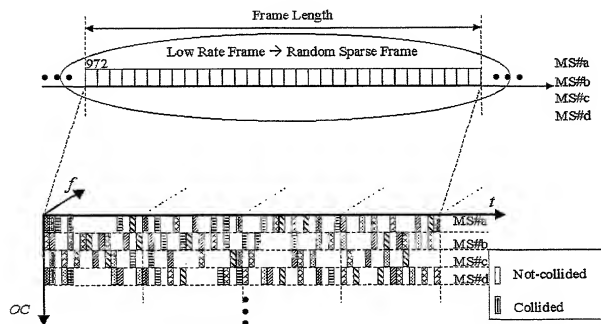


FIG. 14w

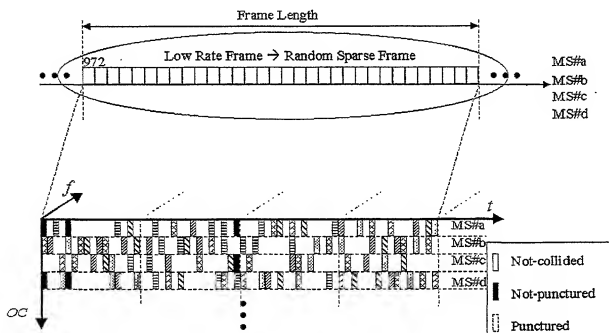


FIG. 14x

44/44

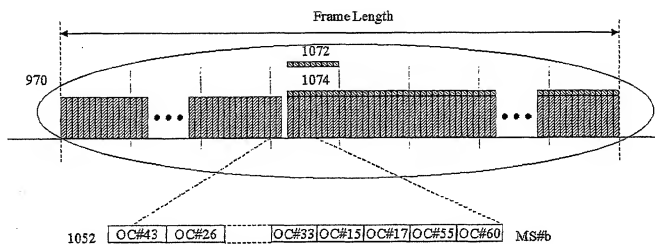


FIG. 15

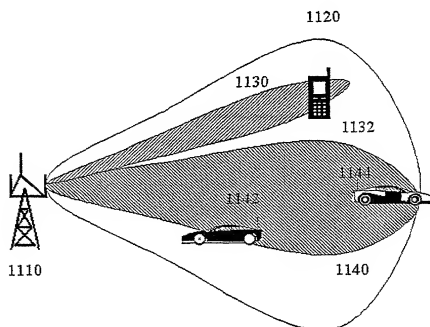


FIG. 16